

**B. Tech. 6th Semester (Electronics & Communication
Engg.) (F. Scheme) Examination, May-2012**

DIGITAL SYSTEM DESIGN

Paper-EE-310-F

Time allowed : 3 hours]

[Maximum marks : 100

Note : Attempt five questions in total, at least one question from each section. Question No. 1 is compulsory. All questions carry equal marks.

1. (a) Define entity with syntax and example 4
- (b) Write a VHDL code for half adder 4
- (c) Differentiate concurrent and sequential statement 4
- (d) Write a short note on PLA 4
- (e) What is CAD tool ? Explain it. 4

Section-A

2. (a) Write the capabilities of VHDL. 10
- (b) What is the operator ? Define its all type. 10
3. Define data types. Discuss its all types in detail. 20

Section-B

4. (a) What is package declaration and package body?
Explain with example. 10
- (b) Write a short note on structural style of modeling. 10
5. Write a short note on any *two* of the following : 10×2
- (a) Process statement
- (b) Functions and procedures
- (c) Case statement with example

Section-C

6. (a) Write a VHDL code for U:/Mux using behavioural style of modeling. 10
- (b) Write a VHDL code for full adder using mixed style of modeling. 10
7. (a) Write a VHDL code for 4-bit up counter. 10
- (b) Write a VHDL code for 4-bit SI SO. 10

Section-D

8. (a) Write a short note on ALU and CPU. 10
(b) Explain the architecture of a simple micro computer system. 10
9. Write short notes on : 4×5
(a) CPLD
(b) FPGA
(c) PAL
(d) PEEL